SURFACE-MOUNT-ENHANCED LEAD FRAME AND METHOD FOR FABRICATING SEMICONDUCTOR PACKAGE WITH THE SAME

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Surface-Mount-Enhanced Lead Frame and Method for Fabricating Semiconductor Package with the Same

FIELD OF THE INVENTION

The present invention relates to a surface-mount-enhanced lead frame and a method for fabricating the semiconductor package with the same, and in particular, relates to a quad-flat non-leaded (QFN) lead frame structure and the semiconductor package utilizing the lead frame and its manufacturing processes.

DESCRIPTION OF THE PRIOR ART

Conventional semiconductor packages use lead frames as die pads to enable the formation of semiconductor packages. The lead frame typically comprises a die pad and a plurality of leads formed around the die pad. After the semiconductor chip is bonded on the die pad and electrically connected to the leads via bonding wires, the chip, die pad, bonding wires and the inner part of the leads are encapsulated by a package body to form the semiconductor package with the lead frame.

There are various structures and types of semiconductor packages using a lead frame as the chip carrier, for example, a quad-flat package (QFP), a quad-flat non-leaded package (QFN), a small outline package (SOP), or a dual inline package (DIP) etc. In order to improve the heating dissipation efficiency of the semiconductor package and while meeting the small size requirement of the chip scale package (CSP), the main stream of semiconductor package is a QFN package with exposed die pad.

As disclosed in US Patent 6,143,981, and referring to Fig. 1A, the characteristics of a quad-flat non-leaded (QFN) package 1 is that there are no outwardly extending leads, thereby the size of the package can be reduced. Further, the bottom surface of the die pad 11 and leads 12 of the lead frame 10 of the QFN package 1, are exposed to the die pad

package body 15, so that the semiconductor chip 13 bonded to the die pad 11 and electrically connected to the leads 12 via gold wires 14 can effectively dissipate the heat generated by the semiconductor chip 13, and the QFN package 1 can be electrically connected to external devices, for example, a printed circuit board (not shown), directly via the exposed surfaces of leads 12. Therefore, the manufacturing processes can be simplified and the production cost can be reduced.

In order to realize high yield, high capacity, precise automation and reduced cost of the packaging process, conventional the manufacturing process of the QFN package 1 is performed in a batch type by using a lead frame module plate which is formed with a plurality of lead frames 10 in matrix. After performing die bonding, wire bonding, molding and singulation processes to the lead frame module plate, a plurality of semiconductor package can be formed.

Referring to Fig. 1B, since the typical material used for lead frame 10 is metallic copper, and in order to effectively solder the lead frame on the printed circuit board, typically a lead frame is pre-plated with a solder metal layer 16 (for example, palladium Pd) on the surface thereof or, after the molding process has completed, electroplated with the solder metal layer 16 (for example, tin/lead Sn/Pb) on the exposed surface of the lead frame 10. It thus allows the lead frame 10 to be effectively soldered on the printed circuit board. However, during surface mounting, since after the singulation process the lead cutting portions 12a of the leads 12 are directly exposed to the ambient, and are usually not covered by solder metal layer 16, such as palladium or tin/lead, oxidation of the metallic copper occurs easily. It thus causes poor wettability and adhesion between the semiconductor package and the printed circuit board. In addition, the lead frame is soldered on the printed circuit board through only the bottoms of the leads 12 in contact with the solder paste 17. Solder joints of the leads 12 and the printed circuit board may be separated due to bad joints or solder openings, since the surfaces of the leads may wet with insufficient tin. This

causes unreliable signal transmission and further affects the reliability of the semiconductor devices.

Referring to Fig. 2, in an attempt to solve the above problems in the prior art, US Patent No. 6,281,568 and 6,455,356 disclose a bent-upward part 21 formed on the ends of a lead frame 20 after the molding process, so as to provide solder paste with larger soldering area to avoid the said problem of insufficient wettability between the leads and solder paste. However, in this manner, the product size is increased, unfavorable to the miniaturization requirements of semiconductor devices. In addition, special mold is needed to bend the externally exposed leads into bent shapes, this not only increases the material costs, but also the chances of poor quality of the bent part such as the peeling off of the bent part.

SUMMARY OF THE INVENTION

A primary objective of the present invention is to provide a surface-mount-enhanced lead frame and a method for fabricating a semiconductor package, so as to increase the lead frame soldering area through simple manufacturing processes, which greatly reduces the problems of signal transmission owing to separation of solder joints and solder openings.

Another objective of the present invention is to provide a surface-mount-enhanced lead frame and a method for fabricating a semiconductor package without increasing the semiconductor package area while efficiently increasing the soldering area of the lead frame and the solder paste, so as to enhance the surface wettability of the lead frame.

A further objective of the present invention is to provide a surface-mount-enhanced lead frame and a method for fabricating a semiconductor package that efficiently increases the soldering area of the lead frame and the solder paste, and enhances the surface wettability of the lead frame without requiring special mold for bending the exposed leads.

To achieve the above and other objectives, the surface-mount-enhanced lead frame of the present invention is provided, which comprises: a die pad and a plurality of leads

disposed around the die pad, wherein a dam bar structure formed with an indentation is formed to be connected to each end of the leads away from the die pad to allow increased wetting surface between the indentation and the solder metal layer at the bottom of the lead frame.

The semiconductor package that utilizes the said surface-mount-enhanced lead frame comprises: a lead frame comprising a die pad and a plurality of leads disposed around the die pad, wherein a dam bar structure formed with an indentation is formed to be connected to each end of the leads away from the die pad; at least a semiconductor chip bonded to the die pad, and electrically connected to the leads; and a package body covering the semiconductor chip and the lead frame in a manner that the indentation of the dam bar structure is exposed to the ambient.

The manufacturing processes of the semiconductor package with the previously disclosed lead frame comprises the steps of: firstly preparing a lead frame module plate which constitutes a plurality of lead frames arrange in matrix-form, wherein any two neighboring lead frames are separated by dam bar structure formed with an indentation, and wherein the lead frame is formed with a die pad and a plurality of leads disposed around the die pad, allowing the dam bar structure to be connected to ends of the leads away from the die pad; bonding at least a semiconductor chip on each of the die pad of lead frames; forming a plurality of conductive components to electrically connect the semiconductor chip to the corresponding leads; forming a package body on the lead frame module plate to cover the lead frames, semiconductor chips, and the conductive components; and performing a singulation process along the indentation to form the semiconductor packages.

Through the surface-mount-enhanced lead frame of the present invention and the method of fabricating the semiconductor package, using simple fabricating methods, an indentation is formed within the dam bar structure separating neighboring lead frames, so that when in the subsequent singulation process of separating individual semiconductor

package with lead frame, the indentation of the dam bar connecting the end of the lead is cut into a first indentation and a second indentation respectively, along the per-determined cutting region between neighboring lead frames. After singulation, it allows the indentation of the same dam bar structure shared by the neighboring lead frames sharing to be connected to the exposed end of the leads, such that when the semiconductor package with the lead frame utilizing the surface-mount-technology is mounted onto an external device, such as a printed circuit board, well wettability and greater soldering areas can be provided to achieve an increase in the soldering area of the solder paste of the lead frame, and signal transmission problems due to separation of the solder joints and solder openings can be greatly reduced by indentation of the dam bar structure at the exposed end of leads. At the same time, under the circumstances that the semiconductor package area is not increased, the soldering area of the solder paste of the lead frame is effectively increased to enhance the surface-mount effect of the semiconductor package with the lead frame.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1A and Fig. 1B (PRIOR ART) are cross-sectional schematic diagrams of the conventional QFN semiconductor package;

Fig. 2 (PRIOR ART) is a cross-sectional schematic diagram of the QFN semiconductor package of US Patent No. 6,455,356;

Fig. 3A and Fig. 3B show a top view the surface-mount-enhanced lead frame of the present invention and its cross-sectional view;

Fig. 4A and Fig. 4B show a top view and a cross-sectional schematic view of the surface-mount-enhanced lead frame of the present invention;

Fig. 5 shows a top view of chip bonding and wire soldering processes performed on the lead frames of Fig. 4A and Fig. 4B;

Fig. 6A and Fig. 6B show a top view and a cross-sectional view of the molding process

performed on the semiconductor structure of Fig. 5;

Fig. 7A shows a cross-sectional schematic view of the singulation process performed on the semiconductor package structures of Fig. 6A and Fig. 6B;

Fig. 7B to Fig. 7D show top views of the singulation process performed on the semiconductor package structures of Fig. 6A and Fig. 6B; and

Fig. 8 shows a cross-sectional view of the semiconductor package soldering to an external device after singulation has completed.

DETAILED DESCRIPTION OF THE PREFFERED EMBODIMENT

Lead frame suitable for quad-flat non-leaded (QFN) package is disclosed in detail in the embodiments of the present invention below. The embodiments of the present invention are provided to illustrate the lead frame suitable for QFN package, thought the lead frame disclosed in the present invention is not limited to this.

Referring to Fig. 3A and Fig. 3B, they are the schematics of the surface-mount-enhanced lead frame of the present invention, however these diagrams are simplified schematics illustratively showing the structural units related to the present invention, the actual lead frame and the semiconductor package layout are more complicated.

The surface-mount-enhanced lead frame 31 of the present invention consists mainly of a die pad 32 and a plurality of leads 33 distributed around the die pad 32, and a dam bar structure 331 formed with an indentation 330 is connected to the end of the leads 33 away from the die pad 32.

The die pad 32 is connected to the lead frame 31 via a plurality of joint shaft 320, and a solder metal layer 36, for example, a palladium or tin/lead alloy, can be covered on the bottom side of the lead frame 31, so as to allow the lead frame 31 employing the surface-mount-technology (SMT) to be mounted onto external devices, such as printed

circuit boards. Through indentation 330 and the solder metal layer 36, good wettability and larger solder area can be provided to enhance the surface-mounting effects.

Referring to Fig. 4 to Fig.7 for a detailed description of the fabrication processes of the semiconductor package with the said lead frame of the present invention.

As shown in Fig. 4A and Fig. 4B, firstly, a lead frame module plate 30 is prepared by method of chemical etching or punching etc. to form a plurality of matrix-form arranged lead frame 31, every neighboring lead frame 31 is separated by a plurality of dam bar structure 331, and which an indentation 330 is formed within, and every lead frame 31 has a die pad 32 and a plurality of leads 33 distributed around the edges of the die pad 32, were the leads 33 are connected to the dam bar structure 331, such that a plurality of package regions are surrounded by of the dam bar structures 331 defined on every lead frame 31. Only two lead frames are illustrated in the Figs., but actually the number of individual lead frames comprising the lead frame module plate is more than that.

The lead frame 31 has a die pad 32 at the center location thereof, and a plurality of leads 33 extending from edges of the lead frame 31 to the center and surrounding the die pad 32, the die pad 32 connects to the lead frame 31 via a plurality of joint shaft 320.

During the process of manufacturing lead frame module plate 30, a mask with opening can be provided in advance on a surface of the lead frame module plate 30, and when in subsequent etching of forming the die pad 32 and leads 33, the indentation can be formed simultaneously on the predetermined dam bar structure 331, or the indentation 330 can be formed by punching method on the dam bar structure 331 of the lead frame module plate 30, the form of the indentation 330 is not limited to the arc curved surface shown in the Figs., but any structure with indentation may be applied to the present invention. Further, since the lead frame module plate 30 is made of copper or iron-nickel alloy material, to effectively solder the lead frame 31 to external device in subsequent processes, a solder metal layer, such as a palladium (Pd) can be formed in advance on the bottom surface of the lead frame

module plate 30.

As shown in Fig. 5, after the said lead frame module plate 30 has been fabricated, die bonding process is then performed to bond at least a semiconductor chip 32 on the die pad 32 of the lead frame 31; and next, wire bonding process is performed to form a plurality of wires, such as gold wires, on the lead frame 31, so that the semiconductor chip 34 can electrically connect the corresponding leads 33 via wires 35.

As shown in Fig. 6A and Fig. 6B, a molding process is further performed, a plastic package body 37 formed on every lead frame 31 by epoxy resin is used to cover the semiconductor chip 34, wires 35, and the upper surface of lead frame 31, but the indentation 330 of the dam bar structure outside the plastic package body 37 is exposed. In addition, after the formation of the plastic package body 37, a solder metal layer 36, such as tin/lead (Sn/Pb) alloy can also be formed on the lower surface of the lead frame module plate 30, so as to provide well wettability between the lead frame 31 and the solder paste.

As shown in Fig. 7A, after that, the singulation process is performed, the lead frame module plate 30 is cut along the predetermined cutting region between the dam bar structures 331 of the neighboring lead frames 331. The process is to place the lead frame 30 built with a plurality of packaged QFN semiconductor packages into a machine (not shown) with a plurality of punching cutting tools 38 to perform punching process. Referring to Fig. 7B and 7C, the punching process uses the punching cutting tools 38 to perform punching in the vertical direction of the respective dam bar structures 331 to separate neighboring leads 33, and punching is performed in the horizontal direction of the dam bar structure 331, the range of punching in horizontal direction should be smaller than the indentation 330 of the dam bar structure 331 to separate the leads 33 connected with the dam bar structure 331. Referring to Fig. 7D, of course, a branched punching tool 38 can be used directly to simultaneously perform punching in the vertical and horizontal direction in order to separate the leads 33 of the lead frames at the same time. By singulation process,

the indentation 330 of the dam bar structure 331 is cut to form a corresponding first indentation 330a and a second indentation 330b, enabling the end of leads 33 of the separated QFN semiconductor package 3 with lead frame connected to a dam bar structure 331 with indentations 330a and 330b, as shown in Fig. 7A.

Referring to Fig. 8, using the surface-mount-enhanced lead frame and the method of fabricating the semiconductor package, a QFN semiconductor package 3 with lead frame is provided, wherein the end of the exposed leads 33 is connected to a dam bar structure 331 with a first indentation 330a and a second indentation 330b, and the surfaces of the first indentation 330a and the second indentation 330b are still covered by a solder metal layer 36 to allow the semiconductor package 3 with the lead frame 31 employing the surface-mount-technology (SMT) to be mounted onto an external device, such as a printed circuit board. Through the surfaces of the first indentation 330a and the second indentation 330b of the dam bar and the solder metal layer 36 covered thereon, well wettability and greater soldering areas can be provided to achieve an increase in the soldering area of the solder paste, and signal transmission problems due to separation of the solder joints and solder openings can be greatly reduced. At the same time, under the circumstances that the semiconductor package area is not increased, this enhances the surface-mount effect of the semiconductor package with the lead frame.

The foregoing embodiments were chosen and described in order to best explain the principles of the invention and its practical application, it is not intended to limit the scope of the present invention in any way, and to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.